Semester	III	Course Title	Digital Electronics	Course Code	18 EC 34
Teaching Period	50 Hours	L – T – P – TL*	3 – 1 – 0 – 4	Credits	4
CIE*	40 Marks	SEE*	60 Marks	Total	100 Marks

CREDITS – 04

Course objectives: This course will enable students to:

- Illustrate simplification of Algebraic equations using Karnaugh Maps and Quine-McCluskyTechniques.
- Design combinational logic circuits.
- Design Decoders, Encoders, Digital Multiplexer, Adders, Subtractors and Binary Comparators.
- Describe Latches and Flip-flops, Registers and Counters.
- Analyze Mealy and Moore Models.
- Develop state diagrams Synchronous Sequential Circuits.

Module – 1

Principles of combination logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique- 3&4 Variables. **(Text 1, Chapter3). L1, L2,L3**

Module -2

Analysis and design of combinational logic: Decoders, BCD decoders, Encoders, digital multiplexers, Adders and Subtractors, Cascading full adder , Look ahead carry, Binary comparators. **(Text 1, Chapter4) L1, L2,L3**

Module -3

Flip-Flops & Its Application: Basic Bistable elements, Latches, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, binary ripple counters, and synchronous binary counters **(Text 2, Chapter6). L1,L2,L3**

Module -4

Sequential Circuit Design: Design of a synchronous counters, Design of a synchronous mod-n counter using clocked T, JK , D and SR flip-flops. **(Text 2,Chapter6)**

Mealy & Moore models, State machine notation, Construction of State diagrams. **(Text 1, Chapter 6) L1,L2,L3**

Module -5

Application of Digital Circuits: Programmable logic devices, Complex PLD, FPGA, Sequential Circuit design- Design of Sequential circuits using ROM’s & PLAs, CPLDs & FPGAs **(Text 3, 9.6 to 9.8,16.4 to 16.6) L1, L2,L3**

Course Outcomes: After studying this course, Students will be able to

- **Acquire** knowledge of Combinational and Sequential logic circuits.
- **Design** the combinational logic Circuits & Sequential Circuits.
- **Analyse** the performance of Synchronous/Asynchronous Sequential Circuits.
- **Design** and Develop Mealy and Moore Models for digital Circuits.
- **Design** of Combinational & Sequential Circuits, and is usuage in digital applications.

Text Books:

- Digital Logic Applications and Design, John M Yarbrough, ThomsonLearning, 2001. ISBN981-240-062-1.
- DonaldD.Givone,—DigitalPrinciplesandDesign‖,McGrawHill,2002.ISBN978-0- 07-052906-9.
- Charles H Roth Jr., -Fundamentals of Logic Design, CengageLearning 5th Edition

Reference Books:

- D.P.KothariandJ.SDhillon,—DigitalCircuitsandDesign‖,Pearson,2016, ISBN:9789332543539.
- Morris Mano, —Digital Design‖, Prentice Hall of India, ThirdEdition.
- K. A.Navas, —ElectronicsLab Manual‖,VolumeI, PHI, 5thEdition, 2015,ISBN:9788120351424.